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Research Article

A Simple Approach for Design and Fabrication of Wilkinson Power Divider on Microstrip Line

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A B S T R A C T

This article deals with the design and fabrication of 1:2 Wilkinson power divider on microwave laminate for DC-10 GHz application. The design is realized on a high quality RT/ duroid laminate having the dielectric constant as 2.33 and strip thickness as 0.787 mm. The relevant design specifications, simulation and the test results are described. The numerical calculations and simulations are performed in Personal Computer Aided Antenna Design (PCAAD) software and the artwork for fabrication is prepared in CorelDraw. A prototype of the design is fabricated and tested on the network analyzer. Some offsets are observed between the theoretical and practical results, which may be attributed to the wide tolerance in the dielectric permittivity specified for the RT/ duroid substrate.

Keywords: Power Divider, Microstrip, Wilkinson, Pcaad, CorelDraw, Microwave

Introduction

In 1960, Ernest Wilkinson, devised a topology for a device that splits a given signal into n signals with equal phase and amplitude and the same device also combines the n divided signals to a single amplified signal (Wilkinson, 1960). During 1965-1975, several modifications are suggested in the basic topology devised by Wilkinson (e.g. Cohn, 1968; Parad and Moynihan, 1965; Ekinge, 1971), however, the fundamental concept remained the same and therefore this easily realized device became famous as n-way Wilkinson power divider. It is widely used in the applications like phased antenna arrays, power amplifiers, signal distribution network etc.

In this paper, a simple cost-effective approach for the design and fabrication of a basic 1:2 Wilkinson power divider on microstrip line is proposed that offers compact low-loss design with high quality factor. After describing the relevant theory of the Wilkinson power divider in section 2, the design specification is presented in section 3, which is then followed by the results and discussion in section 4, that describes the relevant calculations, simulations and the test results of the fabricated power divider.

Theory

A typical Wilkinson power divider is a three-port network device that consists of the quarter-wavelength ($\lambda_G/4$) transmission lines (e.g. waveguides, microstrip or stripline) and suitable resistors in shunt to improve the isolation. The scattering(S) matrix for this three-port device, where port 1 is the input port and ports 2 and 3 are the output ports, is of the form:

Ideally, it has the following three main characteristics (Saleh, 1980; Pozar, 2005):

- **Reciprocity**: It has symmetrical S-matrix elements (Kurokawa, 1965), given by $S_{ij}= S_{ji}$ for all i and j ports.
- **Matched:** It's all ports are matched i.e. $S_{ii} = S_{jj} = 0$.
- **Lossless:** When its input port is excited and the output ports are kept isolated, then it satisfies the relation $[S]^H[S]^* = [I]$, where the superscripts H and asterisk (*) represents the transpose and conjugate of the matrix, respectively and I is the identity matrix.

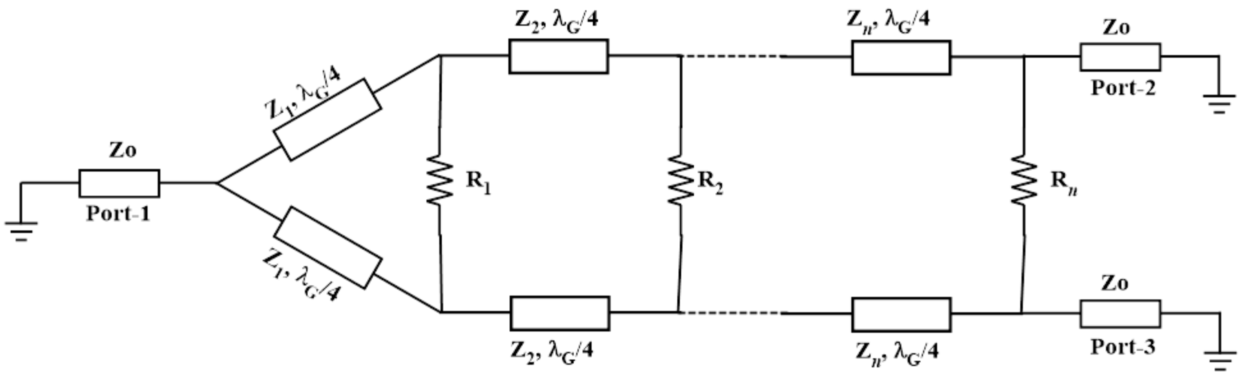

Figure 1.Equivalent circuit of the n-section, three-port Wilkinson power divider

The equivalent circuit of the n-section, three-port Wilkinson power divider is shown in Fig 1. The figure shows the n-pairs of equi-length i.e. parallel quarter-wavelength transmission lines, together with the n resistors R_1, R_2,...R_n in shunt that offers good isolation.

The circuits of the Wilkinson power divider are analyzed using even-odd mode excitations that involves the computation of S-parameters as(Cohn, 1968; Pozar, 2005):

$$[S] = \frac{-1}{\sqrt{2}}\begin{bmatrix} 0 & j & j \\ j & 0 & 0 \\ j & 0 & 0 \end{bmatrix} \qquad (2)$$

Design Specifications

A prototype of the Wilkinson power divider is designed on the microstrip substrate (Fig. 2) with the specification as given inTable 1.As depicted in Fig. 2, the microstrip laminate consists of a conducting strip of width, w and thickness, t, together with a dielectric substrate and a metallic ground plane (Pozar, 2005; Hammerstad and Jensen, 1980).

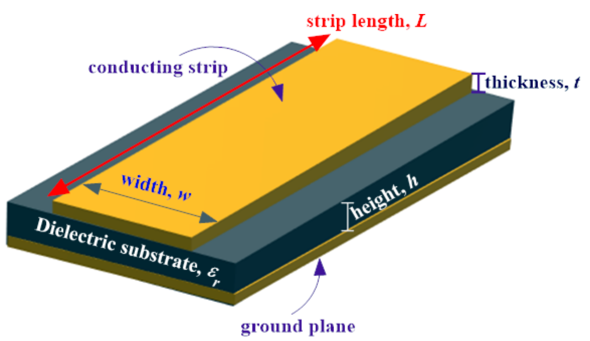

Figure 2.Cross-sectional view of a Microstrip line

Table 1.Design specification

Sr. No.	Parameters	Values
1.	bandwidth	10 GHz
2.	frequency range	DC - 10 GHz
3.	power division	1:2
4.	dielectric constant	2.33
5.	substrate thickness	0.0788 cm

Results and Discussion

Design Calculation and Simulations

At first the effective dielectric constant, ε_{eff} and the line width for the known characteristic impedances are found using PCAAD software (DOS version PCAAD21.EXE) tool developed by Antenna Design Associates, Inc (Kraus, 2001). The known characteristic impedances to be cascaded through microstrip lines taken in the present design are 50Ω, 56.37Ω, 60.255Ω, 65.085Ω, 70.71Ω, 76.82Ω, 82.985Ω and 88.7Ω. Corresponding to these impedances, the ε_{eff}, together with the line widths are obtained using PCAAD on an individual basis, by following the below-mentioned steps:

Step 1: Open PCAAD application software.

Step 2: From the main menu select 'Trans. Lines & Wave guides' (Fig. 3)

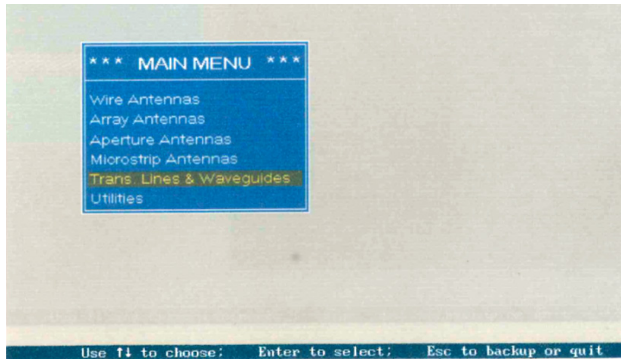

Figure 3.PCAAD Screen Corresponding to Step 2

Step 3: Under the submenu 'Trans. Lines & Waveguides', select 'Microstrip Line' (Fig. 4).

Step 4: Following the previous step, a window will appear (Fig. 5) where the option 'Design (find w)' is selected.

Step 5: In the window that appears after following the step 4, following parameters are to be entered to obtain the effective dielectric constant (ε_{eff}) and the line width. Similar to the case shown for 50 Ω characteristic impedance as shown in Fig. 6, the procedure is repeated for the remaining seven characteristic impedance values. The final ε_{eff} and the line width values obtained from the simulation performed in PCAAD is furnished in Table 2.

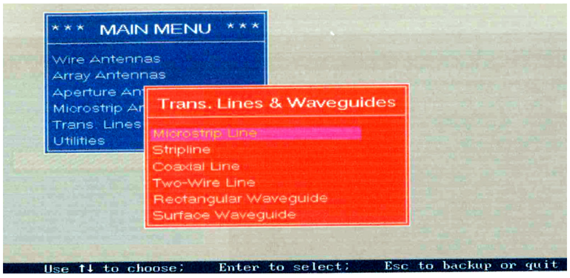

Figure 4.PCAAD Screen Corresponding to Step 3

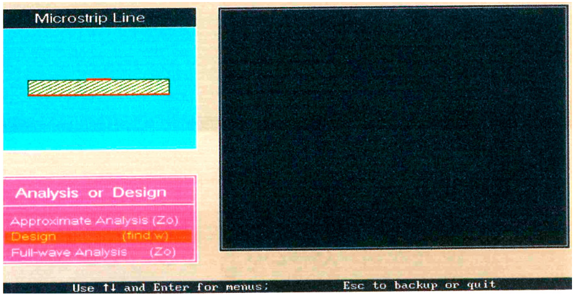

Figure 5.PCAAD screen corresponding to Step 4

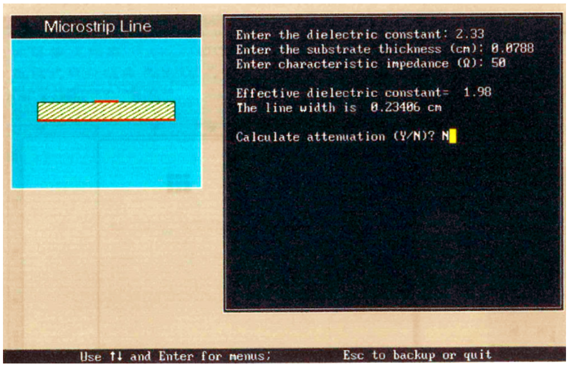

Figure 6.PCAAD screen corresponding to Step 5

9.0 (Fig. 7). While preparing the artwork of the individual transmission lines, values of the line widths up to three significant digits after the decimal point were considered to reduce the errors.

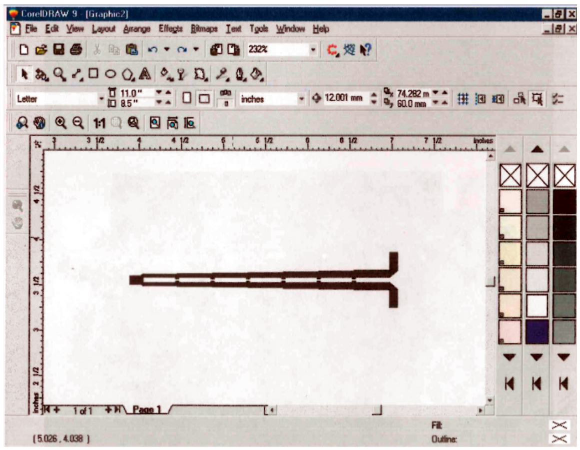

Figure 7.Wilkinson power divider circuit layout in CorelDraw

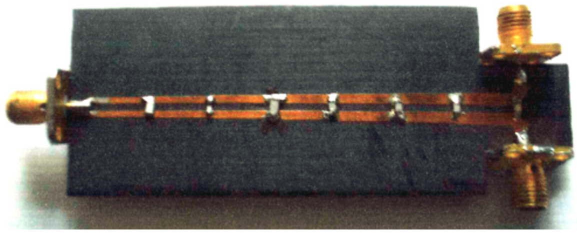

Figure 8.Final fabricated circuit of 1:2 Wilkinson power divider

The design of power divider is realized on a high quality RT/ duroid 5870 laminate (Product Datasheet-1) having ε_r = 2.33 and substrate thickness of 0.787 mm, as shown in Fig. 8. The test and measurement results obtained using network analyzer are tabulated in Table 3.

Table 2.Results Obtained using PCAAD Software

Characteristic Impedance (Ω)	Effective dielectric constant (ε_{eff})	Line width (mm)	Line width (mm) after compensation of +0.015 mm	$\lambda_G/4$
88.7	1.87	0.8684	0.8834	10.969
82.985	1.89	0.9920	1.007	10.910
76.82	1.90	1.1492	1.1642	10.882
70.71	1.92	1.3357	1.3507	10.825
65.085	1.93	1.5424	1.5574	10.797
60.255	1.95	1.7477	1.7627	10.741
56.37	1.96	1.9454	1.9604	10.714
50	1.98	2.3406	2.3556	10.660

Fabrication and test Results

The artwork of the Wilkinson power divider based on the values obtained in Table 2, is prepared in CorelDraw

The operating range of the fabricated power divider is found to have an offset at higher frequency range from the original design value, which could be due to the wide tolerance in the dielectric permittivity specified for the RT/ duroid substrate and the tolerances in the actual chip resistors used in fabrication. In addition, the drifts from the specified values may also be attributed to the test and measurement set-up, calibration of the instruments, mismatch amongst the cables and adapters or errors encountered during etching of the microwave laminate.

Table 3.Test and measurement results of the fabricated Wilkinson power divider

Sr. No.	Parameters	Values
1.	input power	0 dBm
2.	output power at first port	-3 dBm
3.	output power at second port	-3 dBm
4.	range of operation	DC - 7.58 GHz
5.	return loss	less than - 13 dB

Conclusion

A prototype of 1:2 Wilkinson power divider have been designed and fabricated on microstrip line and the performance is evaluated. The performance of the power divider has been checked on the network analyzer. Due to fabrication limitations and losses, the desired operating frequency range have not met, however, by overcoming the fabrication problems the losses can be minimized and the frequency response of the constructed power divider can thus be improved. In addition, the divider is fabricated from low-cost materials, however, the design can easily be customized for high power applications using enhanced components.

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