

Article

A Review on Working Principal and Application of CMOS

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A B S T R A C T

This review paper provide information about basic introduction, working principal, application of CMOS. This paper gives a brief introduction on CMOS, working principal, application, characteristics, advantages & disadvantages. Understanding working principal by using different LOGIC gates.

Keywords: Complimentary, Microprocessor, Immunity, Consumption, Propagation, Noise Margin, Rail, Micro Controller

Introduction

CMOS stands for complimentary metal oxide semiconductor. It is type of MOSFET fabrication process that uses complimentary and symmetrical pairs of P type and N type MOSFETS for logic functions. Complimentary in the sense, it consists of both NMOS and PMOS. Where in NMOS the carriers are electrons and in PMOS the carriers are hole. This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and Application Specific Integrated Circuits(ASICs).

CMOS Working Principle

In CMOS technology, both N type and P type transistors are use to design logic function. The same signal which turns ON a transistor of one type is used turn OFF a transistor of other type. This characteristic allow the design of logic devices use only simple switches, without any need for pull up resistor.

In CMOS logic gates a collection of N type MOSFETs is arranged in a pull down network between the output and the low voltage power supply rail. Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p type MOSFETs in pull up network between the output and the higher voltage rail.

Thus if both a P type and N type transistor have their gates connected to the same input, the P type MOSFET will be ON when the N type MOSFET is OFF, and vice-versa.

For better understanding of CMOS working principle, we will discuss about some CMOS logic gates

CMOS Inverter

The inverter circuit as shown in the figure below. It consists of PMOS and NMOS FET. The input A serves as the gate voltage for both transistors.

CMOS NAND Gate

The below figure shows a 2-input Complementary MOS

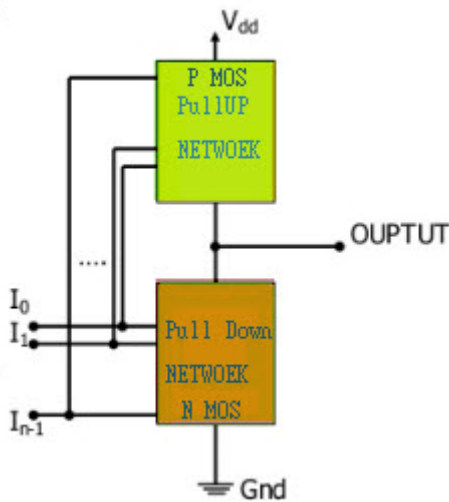


Figure 1. CMOS logic gates using pull-up and pull-down networks

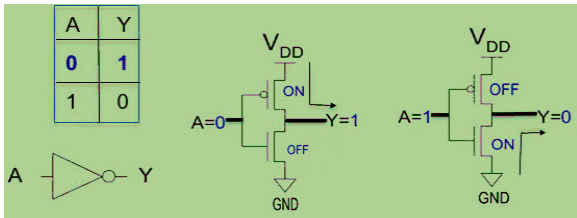


Figure 2. NMOS inverter

NAND gate. It consists of two series NMOS transistors between Y and Ground and two parallel PMOS transistors between Y and VDD.

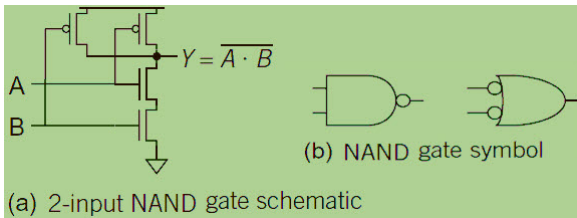


Figure 3. CMOS nand gate

CMOS NOR Gate

A 2-input NOR gate is shown in the figure below. The NMOS transistors are in parallel to pull the output low when either input is high. The PMOS transistors are in series to pull the output high when both inputs are low, as given in below table. The output is never left floating.

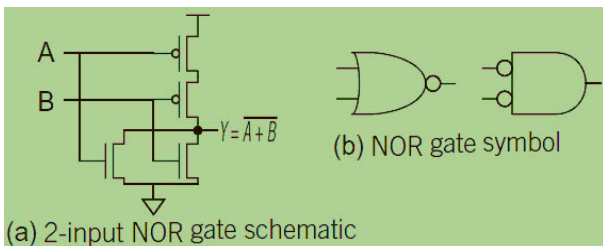


Figure 4. CMOS nor gate

CMOS Applications

Complementary MOS processes were widely implemented and have fundamentally replaced NMOS and bipolar processes for nearly all digital logic applications. The CMOS technology has been used for the following digital IC designs.

Computer memories, CPUs

CMOS has small amount of memory generally used in computer motherboard, main board in order to store BIOS setting. CMOS can also be named as Real time Clock (RTC), CMOS RAM, non-volatile RAM, non volatile BIOS memory.



Figure 5. CMOS on motherboard

Microprocessor Designs

CMOS technology is used for constructing microprocessor, microcontrollers. Basically CMOS is used to make energy efficient CMOS microprocessor. It is used to save the energy and power. The method for saving energy in CMOS is called power gating.

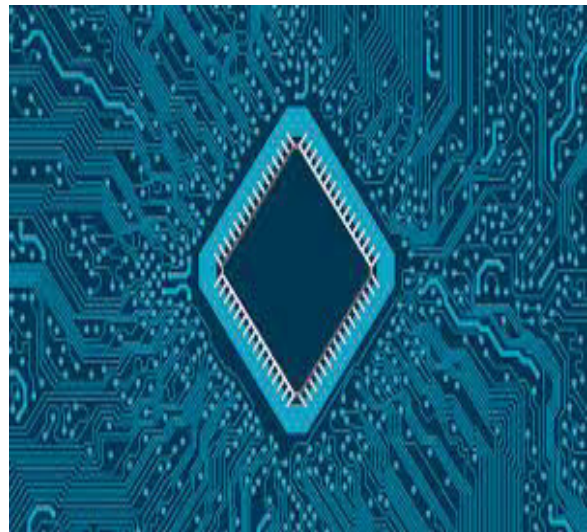


Figure 6. Microprocessor

Flash Memory Chip Designing

All type of memory, including flash memory, have two primary circuit components- the memory array that stores the data, and the logic circuitry that controls how that data moved to, from and within the memory chip.

Although the logic is required for the chip to function correctly, it overhead the reduces how many gigabytes of data can be stored in a given chip area .therefore, the smaller we can make the logic area , the lower cost per gigabyte per our product is. The semiconductor process used to fabricate the logic is called CMOS.

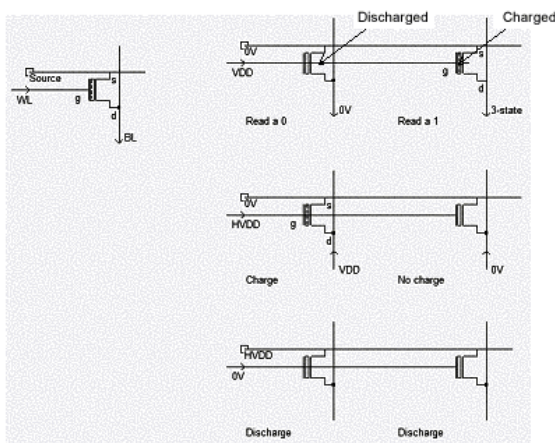


Figure 7. CMOS on memory

Used To Design Application-Specific Integrated Circuits (ASICs)

CMOS is used in ASICs to make the vision chip realization, the important of low cost and low power solution is highlighted.

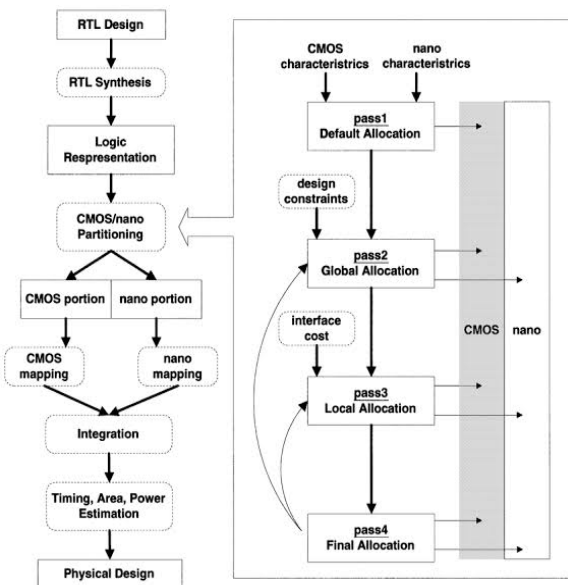


Figure 8. Designing (flow chart)

Characteristics of CMOS

- High noise immunity
- Low static power consumption
- Propagation delay is very less
- High fan out capability

Advantages

CMOS (complementary metal oxide semiconductor) logic has a few desirable advantages.

- High input impedance. The input signal is driving electrodes with a layer of insulation (the metal oxide) between them and what they are controlling. This gives them a small amount of capacitance, but virtually infinite resistance. The current into or out of CMOS input held at one level is just leakage, usually 1 nano Ampere or less
- The outputs actively drive both ways
- The outputs are pretty much rail-to-rail
- CMOS logic takes very little power when held in a fixed state. The current consumption comes from switching as those capacitors are charged and discharged. Even then, it has good speed to power ratio compared to other logic types.
- CMOS gates are very simple. The basic gate is an inverter, which is only two transistors. This together with the low power consumption means it lends itself well to dense integration. Or conversely, you get a lot of logic for the size, cost and power.

Disadvantage

- No bipolar
- Some circuits are not practicable
- Difficult to implement

Conclusion

The use of CMOS is important because NMOS is weak zero strong one device and PMOS is strong one weak zero device , to avoid this problem of leakage current complimentary MOS family is used. In CMOS family logic gates are designed by using both PMOS and NMOS , since function of PMOS and NMOS are compliment to each other, hence it is known as CMOSs family.

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