Journal of Advanced Research in Power Electronics and Power Systems
Volume 7, Issue 2 - 2020, Pg. No. 10-15
Peer Reviewed Journal

Article

Gate Based Variable Gain Amplifier using CMOS Technology

Gaurav Kumar Soni[1], Sonam Gour[2], Monika Tanwani[3]

[1,2,3]Assistant Professor, Arya College of Engineering and Research, Centre, Jaipur.

I N F O

Corresponding Author:
Gaurav Kumar Soni, Arya College of Engineering and Research, Centre, Jaipur.
E-mail Id:
ksoni2709@gmail.com
How to cite this article:
Soni GK, Gour S, Tanwani M. Gate Based Variable Gain Amplifier using CMOS Technology. *J Adv Res Power Electro Power Sys* 2020; 7(2): 10-15.

Date of Submission: 2020-05-01
Date of Acceptance: 2020-05-20

A B S T R A C T

A variable gain amplifier or voltage controlled amplifier is an electronic amplifier or circuit that varies its gain depending on a control voltage. A Variable Gain Amplifier (VGA) based on the gate based design methodology is proposed in this paper. The VGA is designed using the CMOS 90nm technology with 0.35V supply voltage. The gain of the VGA is control or tuned using the control voltage. The power consumption of the VGA cell is achieved 115pW. The proposed VGA cell is cascading to achieve the better response of the VGA, in the cascading four VGA cell is used and the power consumption of the proposed VGA design is 0.95mW. The gain of the VGA is also tuned or varies using the control voltage.

Keywords: CMOS, Amplifier, AGC (Automatic Gain Control), Low Power, VGA (Voltage Gain Amplifier)

Introduction

A variable gain amplifier or voltage controlled amplifier is an electronic amplifier or circuit that varies its gain contingent on a control voltage. The Variable Gain Amplifier (VGA) is one of the critical components in the modern wireless system or modern wireless transceiver designs which are extensively used to recover the transceiver's dynamic range by providing a fixed output power for different input signals. Based on the targeted frequency, Variable Gain Amplifier (VGA) is characterized as high frequency variable gain amplifier for applications with severe bandwidth obligation and over-all determination variable gain amplifier for narrow bandwidth uses. The challenges in Variable Gain Amplifier (VGA) design is mainly the realization of accurate dB-linear typical with minimum power consumption and die area, as well as achieving the obligatory bandwidth for the targeted application.

In the modern wireless communication systems, to maximize the dynamic range, the Variable Gain Amplifier (VGA) is an essential building block. It is also extensively used in disk drives, hearing aids, medical equipment and so on. A Variable Gain Amplifier (VGA) is characteristically working in a response loop to understand Automatic Gain Control (AGC). The variable gain amplifier of an Automatic gain control loop is used to control the power of transmission signal or to correct the amplitude of received signal. There are two thinkable approaches or methods to control the gain of the variable gain amplifier. One is to enterprise a VGA controlled by an analog gain-control signal and the other is to build a discrete gain step VGA with a digital control signal. Fundamentally, digitally controlled VGAs use binary weighted arrays of resistors or capacitors for gain variations while analog-controlled VGAs adopt a variable transconductance or a variable resistance to control the gain. A significant VGA prerequisite is to have a linear-in-decibel gain control characteristic, where the gain of the VGA variations exponentially with the control signal. The exponential gain control is obligatory to accomplish a wide dynamic-range and to preserve the AGC loop settling-time autonomous of the input signal level.

Another important aspect of a wideband VGA is to

attain a large bandwidth. There are many systems for high-speed data communications such as ultra-wideband (UWB) systems, wireless Local Area Networks (LANs), and Bluetooth. These systems provide a high data rate with relatively low power consumption in short-range wireless communications. For high-speed data communication, the bandwidth of a VGA must be very wide. Therefore, a wideband VGA is a key component.[10]

Automatic Gain Control

After a practical point of view, the most general explanation of an AGC system is obtainable in Figure 1. The input signal VIN is enlarged by a Variable Gain Amplifier (VGA), whose gain is controlled by a signal VC. In order to regulate the gain of the VGA to its best output level VOUT, the AGC commonly, first detects the strength level of the signal using the peak detector; it then associates this level with a reference voltage VREF and finally, it filters and generates the required control voltage. This function can be achieved by detecting the signal at the output of the VGA, so the architecture is called "feedback" AGC (Figure 2.1a), or at the input, in which case it is identified as "feed forward" AGC (Figure 1.1b). Both structures contemporary dissimilar inherent physiognomies which means choosing one or the other contingent on the target application. Feedback AGCs The compensations of using feedback AGC are: first, the dynamic range obligatory at the detector input is abridged in the similar way as the AGC gain range; and second, the circuit linearity is high due to the feedback loops' inherent characteristic. On the other hand, this architecture also has the following drawbacks. The high level of feedback required to reach high compression ratios makes feedback processors more probable to exhibition uncertainties if high compression ratios are managed. Instability is also likely in response expanders where high growth ratios are desired. Finally, the feedback loop will always have a maximum boundary bandwidth in order to maintain stability. This maximum bandwidth entails a smallest settling-time. In many uses this is not a noteworthy issue, since several signal periods are processed before the gain is changed. However, in other cases the normal imposes a maximum settling-time that prevents the use of conservative feedback configurations. Furthermore, in order to keep the settling-time constant, the feedback configuration necessitates the use of specific control voltage generation functions. Feed forward AGCs High compression and high expansion ratios are possible with this configuration. Moreover, the feed forward AGC offers a time constant that mostly be contingent on the peak detector response, so this loop is rather not affected by the smallest settling-time restriction. In contrast, the drawbacks of a feed forward AGC are that the level detector is exposed to the entire dynamic range of the input signal and that the loop requires higher linearity, since the feedback loop inherent linearity improvement is now absent. Table 1, summarizes the main characteristics of these two configurations.[6]

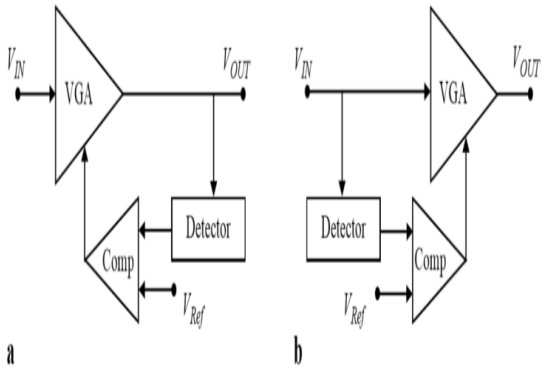

Figure 1.Generation of Electricity

Table 1.Summary of main AGC loop control characteristics

	Advantages	Disadvantages
Feedback Loop	Lower input dynamic range required by peak detector Inherently higher	Instabilities with high compression or expansion Higher settling-time
Feed forward Loop	No instability problems Ideally, zero settling-time	AGC input dynamic range required by peak detector High linearity required in loop

Proposed VGA Design Methodology

The Proposed design of the CMOS variable gain amplifier (VGA) has been achieved in a step by step manner. The overall design is carried out into two parts mainly: - (1) Gate Tuned VGA cell design and (2) 4-cell gate-tuned VGA design.

Topology and Analysis of the Proposed VGA cell

The simplest basic cell consists of a differential pair and is shown in Figure 2.

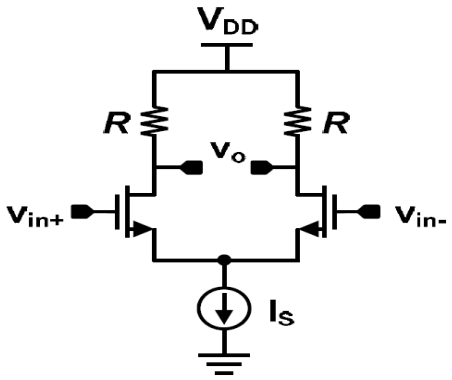

Figure 2.Simplest Basic Cell with a Differential Pair

This is the most conventional differential amplifier with a pair of n-MOS transistors as input and resistors as load. The gain of this differential amplifier is given by:

$$A_V = \frac{V_{out}}{V_{in}} = g_m R \quad (1)$$

In order for the gain to be variable, the resistor R must be variable. Thus it is replaced by a diode-connected MOSFET, which acts like a variable resistor with better accuracy. The small signal impedance of such device is simply $1/g_m$. However, single MOSFET load with resistance $1/g_m$ cannot change the gain as g_m is only related to the drain current I_D, which is determined by the current source and is constant throughout the operation range. Thus, two of such transistor loads are placed in parallel to realize current steering, such that the overall load resistance is variable. The diagram is shown in Figure 3. In Figure 3, one diode connected n-MOS transistor and one p-MOS diode-connected transistor are used for illustration purpose only. They can be of the same type.

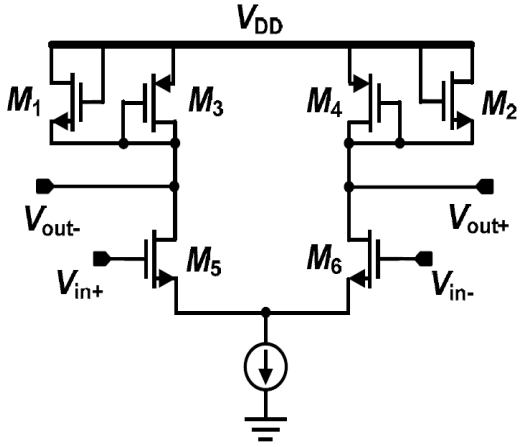

Figure 3.A Differential Pair with n-MOS and p-MOS Active Loads

The small signal equivalent circuit of the load seen by the output node, Z_{LOAD}, is shown in Figure 4. The gain expression is now expressed as:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{g_{m\,5,6}}{g_{m\,1,2} + g_{m\,3,4}} \quad (2)$$

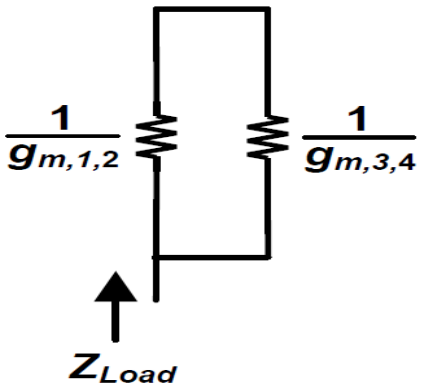

Figure 4.Small Signal Equivalent Circuit of the Load

This is the fundamental structure and expression of the designed VGA cell, and depending on how the control signal is implemented as well as how other techniques are applied, various VGAs suitable for multiple applications can be realized.

Gate-tuned VGA Cell for General Purpose VGA

In order for the gain to be tunable, the control signal must be applied to the circuit. One way to apply the control signal is at the gate of one of the load transistors. The schematic is shown in Figure 5. The reason for not applying complimentary control signal at both gates of the transistors is that one of the transistors must be used to set the DC conditions. The DC operating point should not drift in order to directly cascade multiple cells.

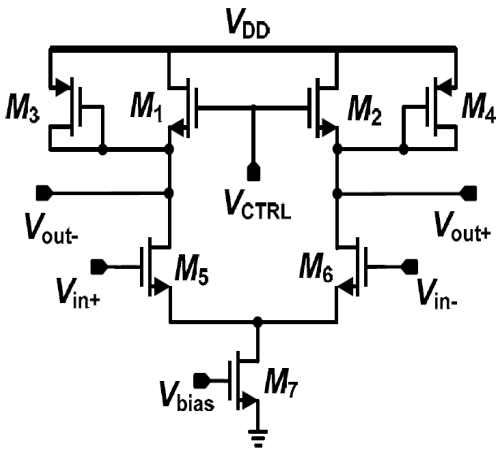

Figure 5.The Gate Tuned VGA Cell

As shown in Figure 5, if the change in g_m can be represented by their respective Δg_m can be rewritten as:

$$A_v = \frac{g_{m\,5,6}}{g_{m\,1,2} + g_{m\,3,4} + \Delta g_{m\,1,2} + \Delta g_{m\,3,4}} \quad (3)$$

The bias condition of the input differential pair transistors M5 and M6 are fixed at all times, thus the current relationship between $I_{DS\,5,6}$, $I_{DS\,1,2}$ and $I_{DS\,3,4}$ can be expressed as:

$$I_{DS\,5,6} = I_{DS\,1,2} + I_{DS\,3,4} \quad (4)$$

And

$$\Delta I_{DS\,1,2} = -\Delta I_{DS\,3,4} \quad (5)$$

As the n-MOS transistors M1 and M2 are biased in the sub-threshold region, the transconductance $g_{m1,2}$ can be expressed as:

$$g_{m\,1,2} = \frac{2I_{DS\,1,2}}{nV_T} \quad (6)$$

Meanwhile, the p-MOS transistors M3 and M4 are biased in the saturation region, and $g_{m3,4}$ can be expressed as:

$$g_{m\,3,4} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_{3,4}} * \sqrt{I_{DS\,3,4}} \quad (7)$$

Differentiating $g_{m1,2}$ w.r.t $I_{DS\,1,2}$ and $g_{m3,4}$ w.r.t $I_{DS1,2}$ gives

$$\Delta g_{m\,1,2} = \left(\frac{2}{nV_T}\right) \Delta I_{DS\,1,2} \quad (8)$$

$$\Delta g_{m\,3,4} = \frac{\mu_p C_{ox}(\frac{W}{L})_{3,4}}{g_{m\,3,4}} * \Delta I_{DS\,3,4} \quad (9)$$

From the above equations we calculate the

$$A_v = \frac{g_{m\,5,6}}{g_{m\,1,2} + g_{m\,3,4} + (\frac{2}{nV_T} - \frac{\mu_p C_{ox}(\frac{W}{L})_{3,4}}{g_{m\,3,4}})\,\Delta I_{DS\,1,2}} \quad (10)$$

As M1 and M2 are biased in the sub-threshold region, the current $I_{DS\,1,2}$ can be expressed as:

$$I_{DS\,1,2} = I_{o\,1,2}\left(\frac{W}{L}\right)_{1,2} \exp\left(\frac{k\,V_{G\,1,2} - V_{S\,1,2}}{n\,V_T}\right) \quad (11)$$

where $I_{o\,1,2}$ is the sub-threshold base current, *k* is the gate coupling coefficient which can be treated as 0.7 throughout the sub-threshold region. Differentiating $I_{DS\,1,2}$ w.r.t $V_{G\,1,2}$ gives the expression of as:

$$\Delta I_{DS\,1,2} = \frac{k}{n\,V_T} I_{o\,1,2}\left(\frac{W}{L}\right)_{1,2} e\left(\frac{k\,V_{G\,1,2} - V_{S\,1,2}}{n\,V_T}\right)\Delta V_{GS\,1,2} \quad (12)$$

The control voltage V_{CTRL} is applied at $V_{G\,1,2}$ which is the gate node of the n-MOS load transistors M1 and M2. The overall gain g_m is close to an inverse exponential function for an appropriate V_{CTRL} range.

Body-tuned VGA cell for general purpose VGA

The other way to apply the control signal is at the body node of the p-MOS transistor. The schematic is shown in Figure 6. The reason for not applying at body node of n-MOS transistor is to avoid the use of deep n-well.

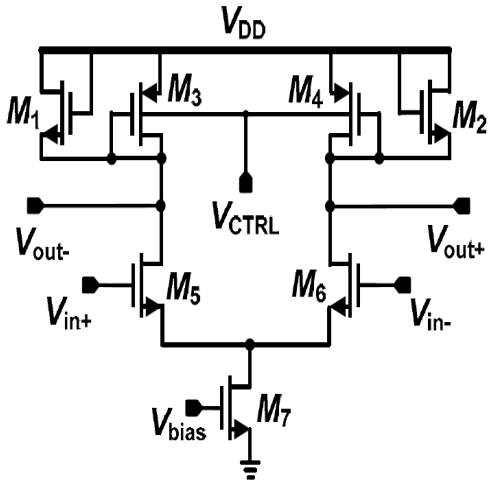

Figure 6.The Body Tuned VGA Cell

In this design, the n-MOS load M1 and M2, are biased in the sub-threshold region, while the p-MOS load M3 and M4 are biased in the saturation region. Thus the change in their transconductance $\Delta g_{m\,1,2}$ and can be expressed as:

$$\Delta g_{m\,1,2} = \left(\frac{2\,\Delta I_{DS\,1,2}}{nV_T}\right) \quad (13)$$

$$\Delta g_{m\,3,4} = \left(\frac{2\,\Delta I_{DS\,3,4}}{V_{OV\,3,4} + \Delta V_{OV\,3,4}}\right)\left(\frac{\Delta I_{DS\,3,4}}{I_{DS\,3,4}} - \frac{\Delta V_{OV\,3,4}}{V_{OV\,3,4}}\right) \quad (14)$$

Now the basic p-MOS I-V equations for M3 and M4 with channel-length modulation neglected can be written as:

$$I_{DS\,3,4} = \frac{1}{2}K_P V_{OV\,3,4}^2 = \frac{1}{2}K_P\left(V_{GS\,3,4} - V_{TH\,3,4}\right)^2 \quad (15)$$

Where

$$K_P = \mu_P C_{ox}\left(\frac{W}{L}\right)_{3,4} \quad (16)$$

The percentage change in is larger than the percentage change in due to their quadratic relationship and of the same polarity. On the other hand, is always much larger than due to their different operation region.

$$\left|\left(\frac{2\,\Delta I_{DS\,3,4}}{V_{OV\,3,4} + \Delta V_{OV\,3,4}}\right)\left(\frac{\Delta I_{DS\,3,4}}{I_{DS\,3,4}} - \frac{\Delta V_{OV\,3,4}}{V_{OV\,3,4}}\right)\right| < \left|\frac{2\,\Delta I_{DS\,3,4}}{V_{OV\,3,4} + \Delta V_{OV\,3,4}}\right| \ll \left|\frac{2\,\Delta I_{DS\,3,4}}{nV_T}\right| \quad (17)$$

Thus we finally get the expression:

$$A_V = \frac{g_{m\,5,6}}{g_{m\,1,2} + g_{m\,3,4} - \frac{2\,\Delta I_{DS\,3,4}}{nV_T}} \quad (18)$$

The threshold voltage with body effect considered can be expressed as follows:

$$V_{TH\,3,4} = V_{TH0} - \gamma_P\left(\sqrt{V_{SB\,3,4} + 2\varphi_F} - \sqrt{2\varphi_F}\right) \quad (19)$$

where V_{THO} is the threshold voltage without considering body effect, γ_P and φ_F are body effect related parameters

Simulatation and Results

In this section deals with simulation results for both the Gate tuned VGA cell and the proposed low power VGA design. The proposed VGA is implemented using the cascading of the four gate-tuned VGA cell in 90nm CMOS technology using LTspice software. The various spice analysis has been done over the circuit for entire VGA in 90nm CMOS environment. In this design Gate tuned VGA is designed.

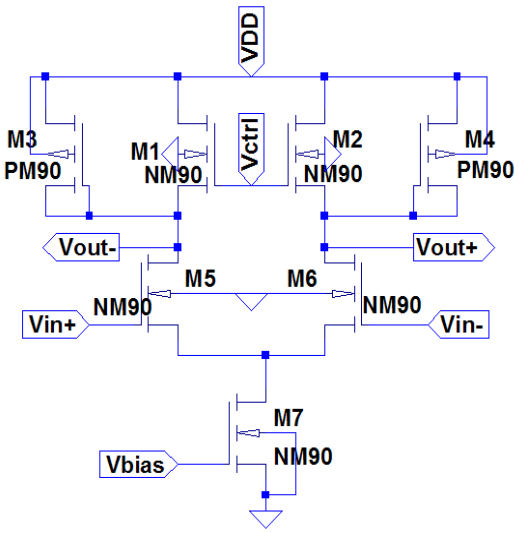

Figure 7.The Proposed Gate Tuned VGA Cell

In this proposed design, four gate tuned VGA cell is cascade. All the simulations and result of the gate tuned VGA cell is

shown below. The proposed design of the gate tuned VGA cell is shown in the fig 7. the power consumption of the proposed gate tuned VGA cell is 112pW, which is very low power consumption of the VGA cell.

The proposed Gate Tuned VGA cell is shown in the figure 7 and the overall output current of the input transistor is shown in the figure 8 and the overall output voltage of the proposed VGA cell is shown in the figure 9.

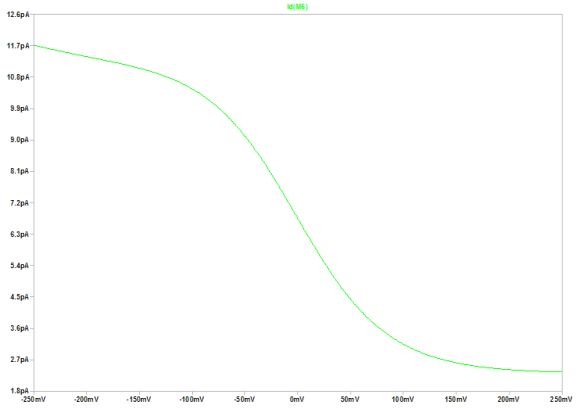

Figure 8.The overall Output Current of Input Transistor

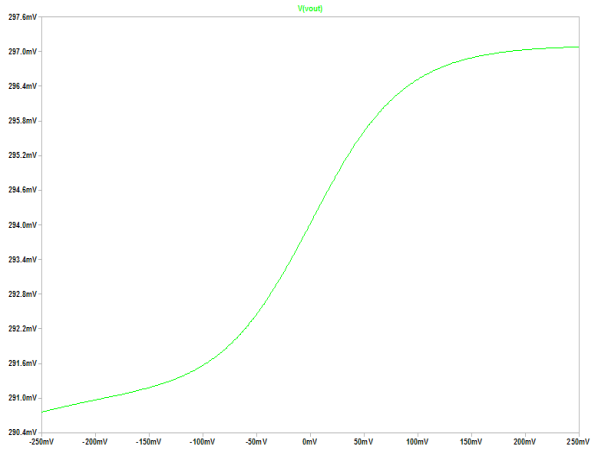

Figure 9.Overall Output Voltage of the Proposed VGA Cell

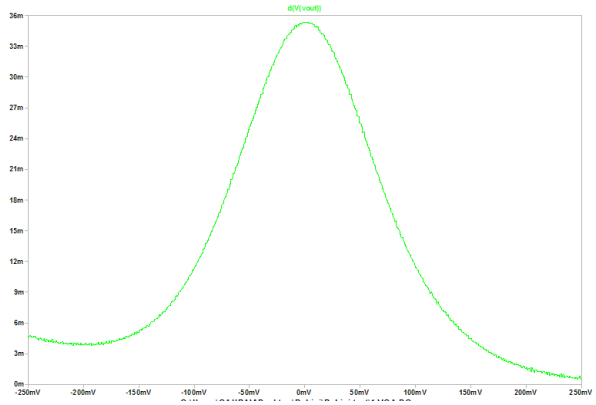

Figure 10.Overall gain of the VGA Cell

Table 2.Transistor Demission of the Proposed VGA Design

Transistor No.	W/L (µm / µm)	Aspect Ratio
M1 , M2, M3, M4	0.18 / 0.09	2
M5	0.1 / 0.09	1
M6	0.09/ 0.18	0.5
M7	1 /0.09	11

Table 3.Summary of VGA Cell Results

Parameters	Value
CMOS Technology	90nm
Supply Voltage	0.35V
Power Consumption	115pW
Gain	36mS
Transconductance Tuning Method	By varying Control Voltage (V_{Ctrl})

In this design four CMOS VGA cell is cascading, is designed using 90nm CMOS technology and the LTspice software is used to simulation. The Proposed Cascading of VGA cell is shown in the figure 11.

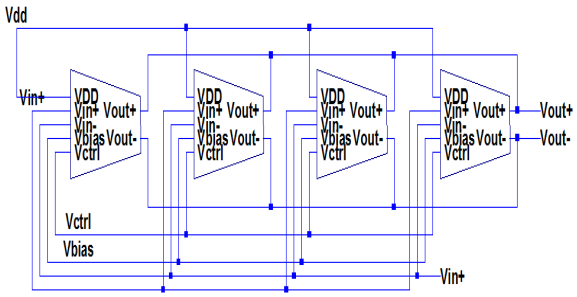

Figure 11.Proposed VGA Cell

The output response of the proposed VGA cell is shown in the figure 12. in this proposed VGA design four VGA cell is cascading.

Figure 12.Output Response of the Proposed VGA Design

Table 4.Summary of Proposed VGA Results

Parameters	Value
CMOS Technology	90nm
Supply Voltage	0.35V
Power Consumption	0.95mW
Transconductance Tuning Method	By varying Control Voltage (V_{Ctrl})

Table 5.Comparison of the Performance of VGA in previous work with proposed work

Reference no.	[2] 2010	[3] 2009	[4] 2009	[8] 2014	[13] 2014	[14] 2010	Current Proposed Work
CMOS Technology (µm)	0.35	0.35	0.18	.065	0.18	0.18	0.09
Supply Voltage (V)	3	3	1.8	1.2	3.3	1.8	0.35
Power Consumption (mW)	5.1	1.7	4.7		31	5.31	0.95
B.W (MHz)	0.80	2.86	30	1200	2000	80	1200
No. STAGE	3	1	3	4	4	1	4

Conclusion

In this proposed VGA cell design the gate based design methodology is used and the proposed VGA cell is cascading with four VGA cell's to achieve the better linearity or better variable gain for the high frequency operation of the VGA. The gain of the VGA is control or tuned using the control voltage. The power consumption of the VGA cell is achieved 115pW with supply voltage of the VGA cell is 0.35V. The proposed VGA cell is cascading to achieve the better response of the VGA, in the cascading four VGA cell is used and the power consumption of the proposed VGA design is 0.95mW. The gain of the VGA is also tuned or varies using the control voltage.

References

1. Razawi B. Design of Analog CMOS Integrated Circuits. Handbook, McGraw-Hill Higher Education, *International edition* 2001.
2. Moro-Frías D, Sanz-Pascual MT, de la Cruz-Blas CA. Linear-in-dB Variable Gain Amplifier with PWL exponential gain control. *IEEE* 2010; 2824-2827.
3. Yuanjin Z, Jiangnan Y, Xu et al. A CMOS VGA with DC offset cancellation for direct conversion receivers", *IEEE Transactions on Circuits and Systems*-I. 2009; 56(1): 103-113.
4. Cortes FP, Bampi S. A 40 MHz 70 dB Gain Variable Gain Amplifier Design Using the gm/ID Design Method. Journal Integrated Circuits and Systems 2009; 7-12.
5. Kar SK, Sen S. A highly linear CMOS transconductance amplifier in 180 nm process technology. *Springer Analog Circuits and Signal Processing* 2012; 163-171.
6. Pérez JPA. AGC Fundamentals. *Springer Analog Circuits and Signal Processing* 2011; 13-28.
7. Zhiming C, Yuanjin Z, Chung CF et al. A Low-Power Variable-Gain Amplifier With Improved Linearity: Analysis and Design. *IEEE Trans. Circuits Syst.* I2012; 59: 2176-2185.
8. Lu Z, Ma K, Yeo KS. A 1.2-GHz bandwidth variable gain amplifier with continuous dB-linear control in 65nm CMOS. *IEEE* 2014;1-4.
9. Ravindran A, Vidal E, Yoo SJ et al. A Differential CMOS Current-Mode Variable Gain Amplifier with Digital dB-Linear Gain Control. *Analog Integrated Circuits and Signal Processing* 2004; 38: 161-174.
10. Zheng Y, Yan J, Xu YP. A CMOS dB-linear VGA with pre-distortion compensation for wireless communication applications. *IEEE*, I : 813-16.
11. Song WC, Oh CJ, Cho GH et al. High frequency/high dynamic range CMOS VGA. *IET Digital Library* 2000; 36(13): 1096-109822.
12. Sun Z, Yan Y. Design of a 2 GHz Linear-in-dB Variable-Gain Amplifier with 80-dB Gain Range. Hindawi Publishing Corporation Active and Passive Electronic Components 2014; 1-7.
13. Jiajie Z, Taishan Ma, Chengyan Ma et al. A novel reconfigurable variable gain amplifier for a multi-mode multi-band Receiver. *Journal of Semiconductors* 2010; 31(7): 1-6.