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Article

Impact of Interconnect Variation on Ultra Low Power Clock System

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A B S T R A C T

By virtue of high component density and enhanced performance state-of-the-art integrated chips, power density has increased considerably. Increased power consumption deteriorates the performance, endangers the reliability and increases the packaging cost and therefore power consumption has emerged as a forefront design metric. An attempt to reduce the power consumption hampers the overall performance and robustness of the system. All these factors viz power, reliability and performance of a digital synchronous system are significantly influenced by the clock system and therefore design of low power and robust clock system becomes obvious. For moderate and low frequency applications having stringent power budget, sub threshold circuits satisfies the demand of ultra-low power. However, due to exponential V-I characteristics, robust design is a critical concern in sub threshold regime. Furthermore, high component density and increased complexity leads to increased wire density. Therefore, along with the challenges posed by performance degradation and PVT variability of device in sub threshold, there is need to investigate the impact of interconnect variation on clock system performance parameters in this regime. This paper therefore, explores the impact of variation in interconnect parameters in buffered as well as unbuffered CDN of low power clock system.

Keywords: Ultra-Low Power, H-tree CDN, Variability, Sub Threshold

Introduction

The unprecedented success of Semiconductor, by virtue of technology scaling in each new generation, have led to the development of Complementary Metal Oxide Semiconductor (CMOS) integrated circuit at a very fast pace.[1] The electronic systems have been shrinking and system on chip has become vital for the emerging portable applications. But this has increased the power density and hence to get rid of the performance degradation due to excessive power dissipation, power management has become an integral part of design flow. Researchers have suggested various method such as voltage scaling, switching activity reduction, architectural techniques like pipelining and parallelism to reduce the power consumption but lowering the supply voltage is the most popular method to achieve low power since it quadratically reduces the dynamic power consumption.[2] Thus supply voltage,V_{DD}, can be reduced till the point when leakage power consumption outweighs the dynamic energy savings.[3,4]The extreme case of V_{DD} reduction is to reduce it below threshold voltage called as sub threshold operation which quench the ultra-low power (ULP) demand but at the cost of increased delay and variability.[5,6] Multitude of applications such as pace maker, RFID tags, wrist watches, biomedical sensors and wireless sensors have moderate speed requirement and

are bounded by ULP budget. Low power consumption is an essential requirement for such applications since battery charging or replacement is infeasible. These applications incorporate digital signal processing and communication systems to collect and communicate the data. Clock system, comprising of clock generator and clock distribution network (CDN), is most power consuming but a vital building block for such applications. Therefore for prolonged battery life, challenges in designing low power clock system needs to be investigated.

Sub threshold circuits are the best alternative to achieve low power but the major challenge in working in this region is to reap the advantage of ULP benefits with minimal degradation of speed & robustness. The second major challenge for sub threshold region involves designing a functional and practical interconnect. Although the number vary from design to design, FPGA typically dissipate 60-70% of their power in the interconnect network (wires, connection boxes, routing switches and buffers), 10-20% in clock network and 5-20% in logic.[7]This breakdown indicates that a focus on interconnect performance in Clock Distribution Network (CDN), which is network of wires, is necessary. This paper therefore explores the impact of variation in interconnect parameters on performance parameter of clock system.

The rest of the paper is organized as follows: Section II describes the sub threshold operation of silicon Mosfet. The related work is reviewed in Section III. Section IV describes the basics of CDN. Section V analyses the impact of process variation in interconnects on clock system parameters followed by conclusion in section VI.

Weak Inversion(WI) Region

Biasing the transistor in the Weak Inversion (WI) region is the best design approach to minimize the power consumption as reported by the researchers.[2] In sub threshold (or WI) operation, the supply voltage of transistor is kept below threshold voltage. The threshold voltage is given by

$$V_{th} = V_{tho} + \gamma(\sqrt{|\phi_s + V_{SB}|} - \sqrt{\phi_s}) \quad (1)$$

$$V_{tho} = V_{FB} + \psi_0 + \gamma\sqrt{\psi_0} \quad (2)$$

Where, Vbs is the source-bulk voltage, V_{th0} is the threshold voltage for Vbs = 0, γ is body effect factor, ϕs is surface potential, Ψ_O is surface potential and VFB is the flat band voltage.[8]

The temperature dependence of threshold voltage is modeled as

$$V_{th} = V_{tho} - KT \quad (3)$$

In Weak Inversion(WI) operation, the drive current I_{DS} is dominated by the diffusion current in contrast with conventional operation of CMOS circuit where drift current is dominant factor in contributing $I_{DS.}$ The sub threshold leakage current given by equation (4), acts as a driving current in sub threshold operation.[9]

$$I_D = I_0 e^{\frac{(V_{GS} - V_{th} + \eta V_{DS})}{nV_T}} (1 - e^{\frac{-V_{DS}}{V_T}}) \quad (4)$$

Where, $I_0 = \mu_0 C_{ox} \frac{W}{L}(n-1)V_T^2$ (5)

Is the drain current at $V_{GS} = V_{DD} = V_{th}$

is the carrier mobility, C_{OX} is the gate-oxide capacitance, $U_T=(k_BT/q)$ is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge, V_{th} is the threshold voltage of the MOSFET, and *n* is the subthreshold slope factor, η is the DIBL coefficient. DIBL is the only important SCE among other SCE's like velocity saturation in transistor operated in the WI region.[9]

The right term in equation (4) models the roll-off current that occurs when V_{DS} drops to within a few times U_T.

Due to exponential I-V characteristics in the sub threshold region, the devices have a high trans conductance gain and thus near-ideal Voltage Transfer Characteristics (VTCs). On one hand this exponential characteristics facilitates in implementing widely tunable circuits, on the other hand this characteristics makes the circuits prone to PVT variations in this regime.

Basics of Clock Distribution Network

The Clock Distribution Networks (CDNs) are used to distribute clock signal. The global clock, if not distributed across the chip such that it reaches all of the clocked elements at nearly the same time, would lead to a clock skew between physical clocks that are near and far from the clock generator.[10] CDN can significantly affect the overall system performance and reliability since the performance of a VLSI system is usually determined by its clock frequency.[11] Thus, while designing the clock distribution system utmost care must be taken to equalize the time between the clock generator and the clocked receivers. Global clock distribution networks can be classified as grids, H-trees, spines, ad hoc, or hybrid. A specific topology can be opted for a specific application as per its requirement to reduce the skew.[10] Further, various factors such as the systematic or random process variations, interconnect layout-dependent coupling effects, on-chip inductance effects; IR-drop, etc. have a large impact on the performance of a clock distribution network. With technology scaling, the global interconnects becomes more resistive leading to larger delays, increased skew and reduced performance. Variability is another major problem posed by technology scaling. The unpredictable behavior of this wire dominated CDN due to process and temperature makes CDN design

more critical. Consequently, as a result of PVT variations, the clock signal can have both spatial (skew) and temporal (jitter) variations leading to performance degradation and circuit malfunction.[12] Unfortunately, as chips are getting larger, wires are getting slower and clock loads are increasing. In this scenario, the distribution delay tends to go up even as cycle times are going down. Good clock distribution networks can achieve low systematic skews, which were dominant component in the past, but random, drift and jitter components are becoming an increasing fraction of the cycle time. H-tree with numerous clock buffers is a commonly used topology to have identical timing characteristics. However, the H tree topology of CDN exhibits the sensitivity to process and environmental variations. Therefore in this paper the impact of process variation in both buffered and unbufferd H-tree CDN is investigated.

Related Work

Conventionally researchers have proposed numerous techniques to minimize clock skew, slew, power consumption such as driver sizing, repeater insertion, interconnect width optimization, pulsed signaling, dynamic drivers, current mode circuits, adding cross links, non tree CDN etc.[13-20] Researchers in[20] have suggested the technique of selectively changing the bulk polarizations of the clock buffers to minimize the clock-skew variations due to thermal gradients on temperature-sensitive CDNs. Both ABB and FBB cases have been discussed.

The applicability of conventional techniques to sub-threshold domain needs to be investigated. The authors in[21] after performing rigorous analysis concluded that incontrast to s uper threshold, repeater insertion in global interconnect will further increase the delay as well as switching energy. J. Tolbert X. Zhao, S. K. Lim, S. Mukhopadhyay[22] devised a technique of dynamic nodal capacitance to control clock slew while minimizing the energy for sub threshold CDN. The authors recommended that tighter nodal capacitance is essential to control the slew in sub-threshold CDNs. But clock skew and latency were not taken into consideration. J. Kil et al.[23] explored gate voltage boosting technique to improve the sub-threshold interconnect performance and robustness.

The parasitic effects introduced by the wire have gain significant importance with technology scaling. The CDN performance in clock system depends on this wire parasitic and therefore an analysis of role and behavior of interconnect wire in CDN needs to be investigated. Furthermore, the lateral and vertical dimension variation in interconnect brings about variation in wire parasitic causing clock latency and skew to vary across the chip. With increased wire density in VLSI chip, the impact of variation in width and spacing brought about by lithography and etching process also need to be investigated. This paper therefore explores the impact of variation in interconnect parameters in CDN on performance parameter of clock system CDN at different supply voltages ranging from 0.9 V to 0.2V.

Variability analysis of H-tree CDN

Process variation is the important issue at lower technology nodes which is exacerbated with reduction in power supply. The capacitive, inductive and resistive parasitic introduced by wire have significant impact on performance and reliability of conventional circuits. This section explores variability performance of buffered as well as unbuffered H tree CDN. Fig 1&2 depicts the clock system with buffered and unbuffered H-tree.

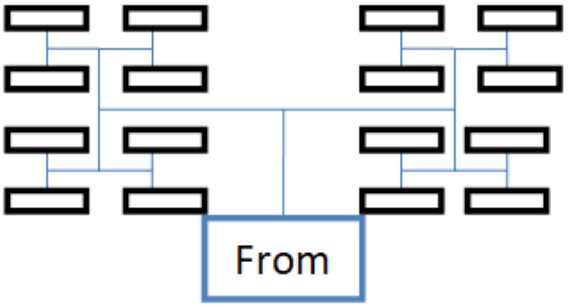

Figure 1.Clock System with unbuffered H tree

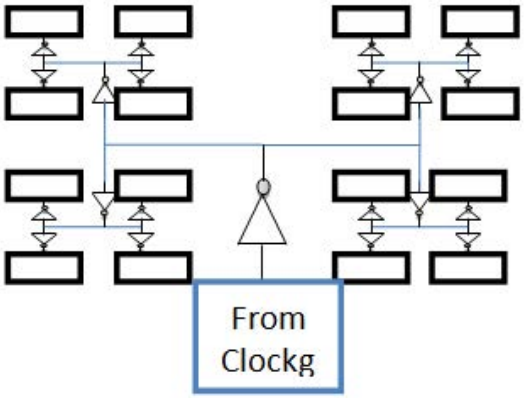

Figure 2.Clock System with buffered H tree

A two level H tree CDN circuit is simulated at 32nm technology node using PTM model.[24] The equivalent RLC model for CU interconnects is shown in Figure 3. The RLC parameters of Cu interconnect are extracted from PTM tools[24] for Cu interconnects.

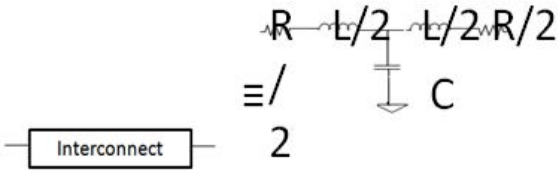

Figure 3.RLC model for CU interconnect

The resistance of wire is given by;

$$R = \frac{\rho\, l}{t\, w} 6 \quad (6)$$

Where ρ is the resistivity, w, are the width, length and thickness of wire respectively. Thus, the resistance is inversely proportional to thickness and width.

The capacitance of wire is given by

$$C = \varepsilon_{ox} l \left[\frac{w}{h} + 0.77 + 1.06 \frac{w}{h^{0.5}}^{0.5} + 1.06 \frac{t^{0.5}}{h^{0.5}} \right] \quad (7)$$

The total capacitance of wire given by equation 9 is the sum of parallel plate capacitance and fringing capacitance. The fringing component of capacitance is directly proportional to thickness of wire.

However, inductor role becomes dominant only when switching speed is high.

The variation in dimension of wire, brought about by process variation, is reflected in variation of its parasitic components which in turn leads to variation in latency, fall time and slew in clock system. In order to investigate the impact of width variation of interconnect on clock system performance parameter, width (W) is changed (increased and decreased by 10%) and the observation reveals that for buffered tree the fall time, slew and latency are deviated only by 2-3% from the nominal value by increase in width at 0.9 Also slew and latency are not affected significantly for decrease in width at 0.9 V, but fall time is increased by 18.9% with decrease in width at 0.9V. The clock parameters don't show significant deviation from nominal conditions at 0.2V supply voltage for both increase and decrease in width.

To analyze the impact of thickness variation of interconnect on clock system performance parameter, thickness (T) is changed (increased and decreased by 10%) and the results for buffered tree shows that decrease in thickness don't deviate the clock parameters prominently at 0.9V. Slew and latency are not affected much, however increase in thickness increases the fall time by 12.4% at0.9V supply. The clock parameters almost remain same at 0.2V supply voltage for both increase and decrease in thickness.

Likewise, the spacing variation impact on Clock parameters is investigated by varying spacing by 10% for buffered tree and the results shows that with increase in spacing changes the fall time by 11.1% at 0.9V.Slew and latency are changed only by 4-5%.With decrease in spacing fall time increase by 20% and slew by 12.7% at 0.9V. The clock parameters show a very small deviation from nominal conditions at 0.2V supply voltage for both increase and decrease in spacing for buffered tree.

The variation in width, thickness and spacing causes variation in both resistance and capacitance. These wire parameters dominate the relevant metrics of clock circuit like slew and fall time in super threshold region for buffered CDN as depicted in Figure 4 to Figure 9.This is because with technology scaling, device becomes faster but wire shows opposite trend. As supply voltage is scaled down, the device resistance increases and therefore resistance of interconnect becomes negligible in deep sub threshold region and therefore slew and fall don't show significant variation at 0.2V. The CDN delay from clock source through H network to the clocked elements is called as latency. Also, variation in W, T, or S of interconnect parameters don't have significant impact for buffered H-tree at lower voltages as seen from Figure 10 to Figure 12. Since latency is mainly affected by the resistance of wire and buffer. The device resistance is dominating factor in sub threshold whereas interconnect resistance mainly decides the latency in conventional super threshold circuits. Therefore slight variation in latency is observed for higher voltages but for lower voltages the plot of latency variation versus W, T and S nearly overlaps. However, variation in interconnect parameters have significant impact on skew at lower supply voltages as evident from Figure 13 to Figure 15

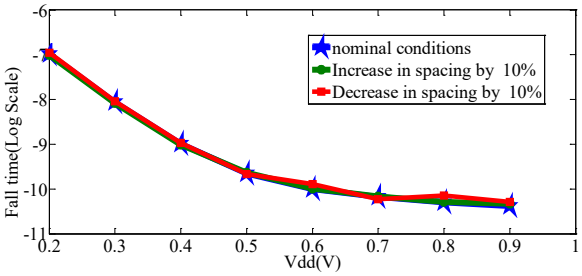

Figure 4.Variation of fall time with space variation in buffered H tree

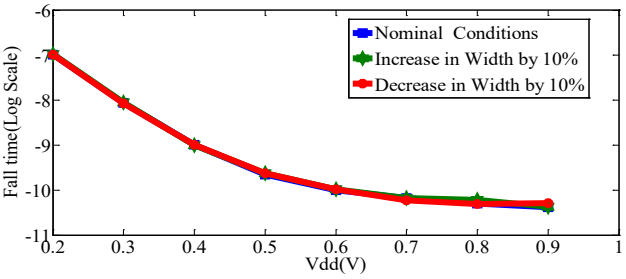

Figure 5.Variation of fall time with width variation in buffered H tree

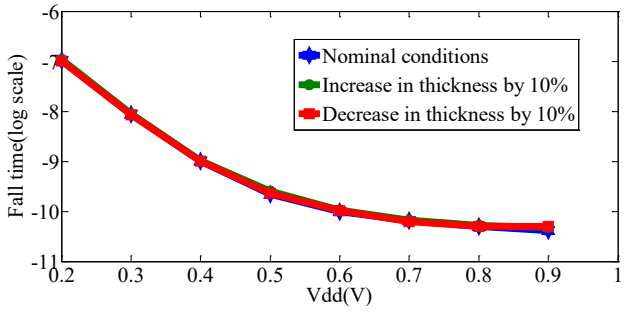

Figure 6.Variation of fall time with thickness variation in buffered H tree

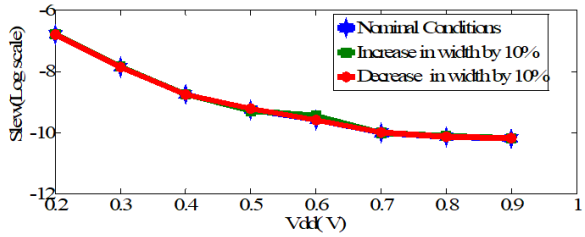

Figure 7.Variation of slew with width variation in buffered H tree

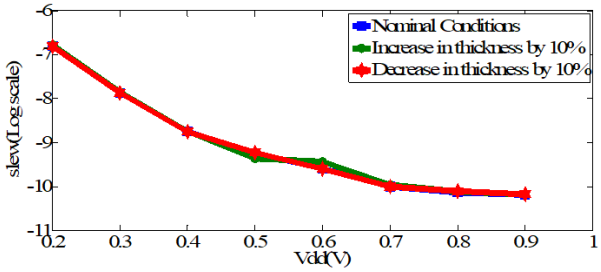

Figure 8.Variation of slew with thickness variation in buffered H tree

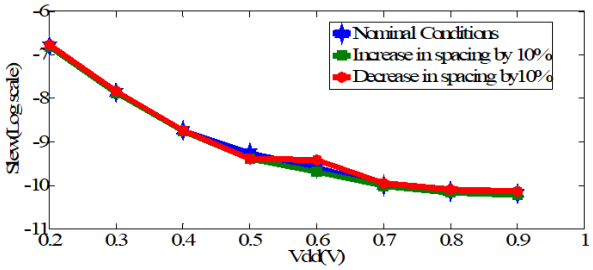

Figure 9.Variation of slew with spacing variation in buffered H tree

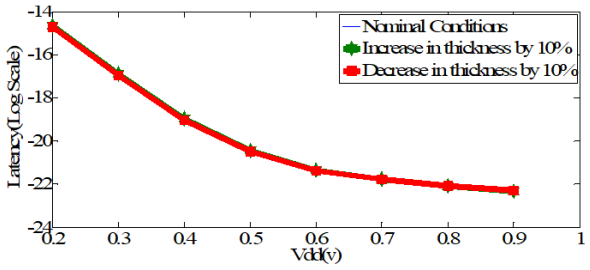

Figure 10.Variation of latency with thickness variation in buffered H tree

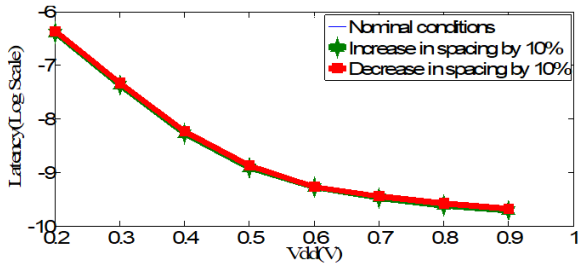

Figure 11.Variation of latency with spacing variation in buffered H tree

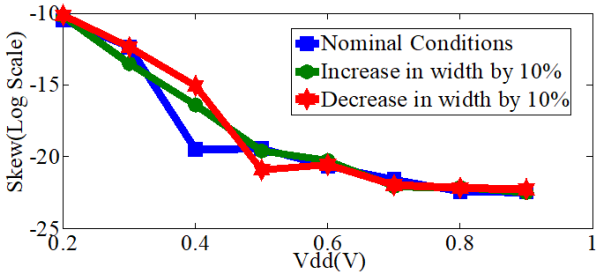

Figure 13.Variation of skew with width variation in buffered H tree

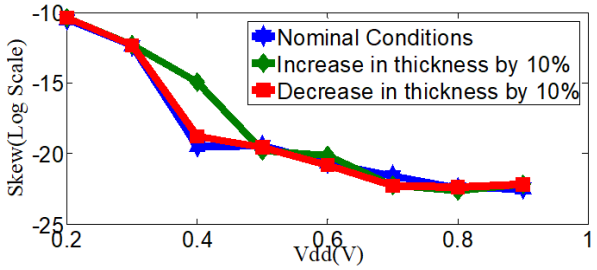

Figure 14.Variation of skew with thickness variation in buffered H tree

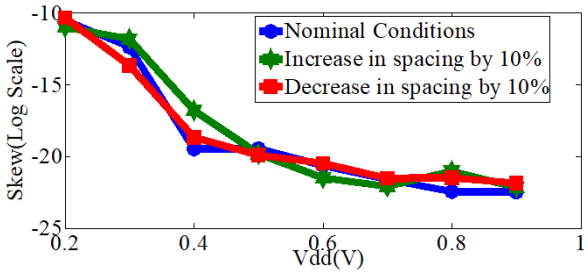

Figure 15.Variation of skew with spacing variation in buffered H tree

Large central drivers are used to drive the unbuffered tree in simulation set up in such a way that both buffered and unbuffered clock system satisfy the slew and skew constraint and have comparable power consumption.

In order to verify how the clock parameters vary with interconnect parameter variations for clock system with buffered tree, W,T,S was changed by 10% and deviation in clock parameters was noted. With increase in width by 10% fall time, slew and latency changes by 8.36%, 6.64% and 6.09% respectively and with decrease in width by 10%, these parameter changes by 4.5%, 1.52% and 8.11% respectively at 0.9V. At 0.2V, fall time and slew are deviated by 1-2%only for both increase and decrease in width. However latency is changed by 5.24% and 21% with increase and decrease in width respectively.

With increase in thickness nominal deviation is observed for fall time, slew as well as latency at 0.9V.With decrease in thickness latency changes by 7.05%, slew and fall time are not changed significantly at 0.9V.Slew and fall time both don't show any significant variation with increase as

well as decrease in thickness at 0.2V, however latency is changed by 10.3% and 8.78% respectively for increase and decrease in thickness respectively.

Similarly increase in spacing don't change the fall time, slew and latency significantly, however decrease in spacing changes these parameters by7.7%,7% and6.69% respectively at 0.9V. At 0.2V latency is changed by 12.6% and 19.4% for increase and decrease in spacing respectively. Fall time and slew are deviated by 4-5% from nominal conditions for both increase and decrease in spacing.

The parameters like slew and fall time are not affected significantly, as evident from Figure 16 to 21, with interconnect variation implying that the these parameters are mainly governed by the clock drivers rather than interconnect.

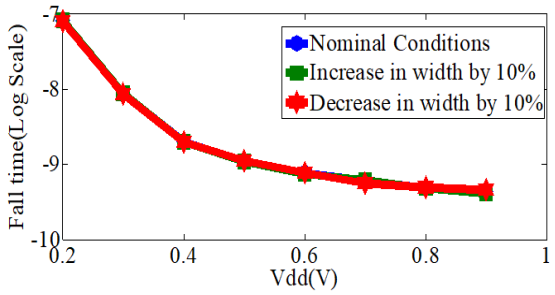

Figure 16.Variation of fall time with width variation in unbuffered H

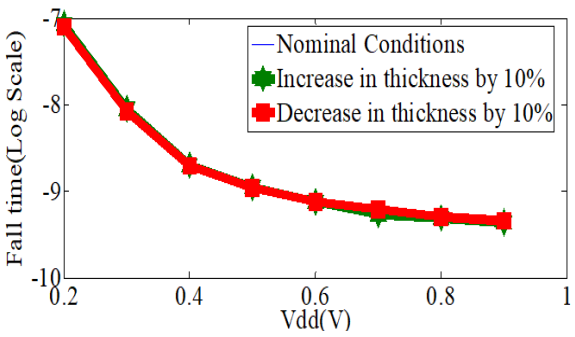

Figure 17.Variationof fall time with thickness variation in unbuffered H tree

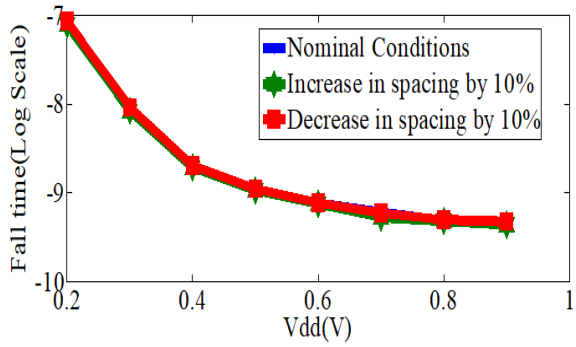

Figure 18.Variation of fall time with spacing variation in un buffered H tree

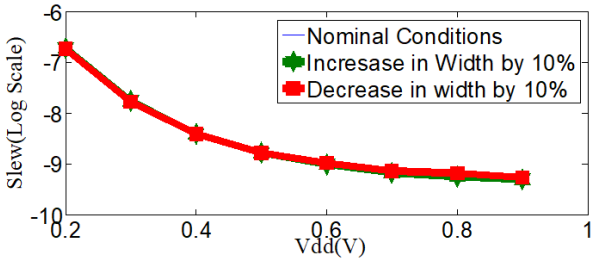

Figure 19.Variation of slew with width variation in unbuffered H tree

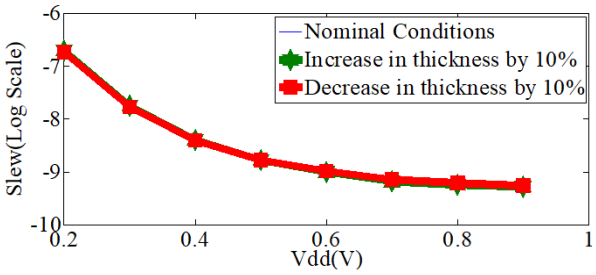

Figure 20.Variation of slew with thickness variation in unbuffered H tree

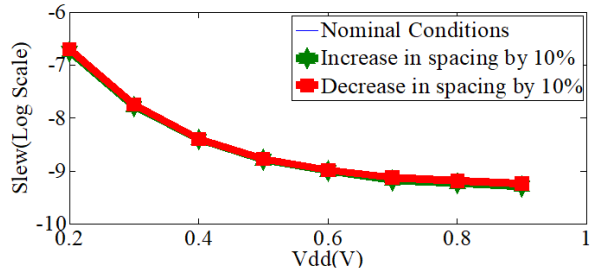

Figure 21.Variation of slew with spacing variation in unbuffered H tree

Since no buffers are available in unbuffered tree, it is the interconnect resistance which decides the latency. Therefore variation in latency is observed in the unbuffered tree under altered conditions in contrast to buffered tree as can be seen from Figure 22 to Figure 24.Variation in interconnect parameter have significant impact on skew of unbuffered tree as evident from Figure 25 to Figure 27.

Finally, the overall impact of variation in all three parameters of interconnect viz. W, T, S by 10% is analyzed. For buffered tree , fall time changes by 4.16 % and 21.73% for increase and decrease in W,T, S resp., Slew changes by 4.02% and 11.8% for increase and decrease in W,T,S resp. and latency changes by 6.86 and 8.52% for increase and decrease in W,T,S respectively at 0.9V. No significant change is observed in the clock parameters with deviation in W,T and S at 0.2V for buffered tree with variation in interconnect parameters.

It is observed that for unbuffered tree clock system fall time changes by 7.28% and 14.4% for increase and decrease in W,T, S resp., Slew changes by 17.77% and 13.6% for increase and decrease in W,T,S resp. and latency changes by 20.55 and 18.18% for increase and decrease in W,T,S

respectively at 0.9V.No significant change is observed in the clock parameters with deviation in W,T and S at 0.2V except latency which changes by 27.87% with decrease in W,T,S .

As can be seen from Figure 28 and Figure 29 unbuffered CDN proves to be more robust compared to buffered tree at higher voltages for parameters likes slew and fall time. However, at lower voltages interconnect variation does not have significant impact on these parameters for both buffered as well as unbuffered tree. Latency with buffered tree increases significantly with decrease in supply voltages for buffered clock tree whereas it remains almost constant for unbuffered CDN. Figure 30 depicts the variation in latency for buffered and unbuffered tree under nominal conditions and with W,T and S variation. Significant variation in latency is observed in the unbuffered tree under altered conditions.

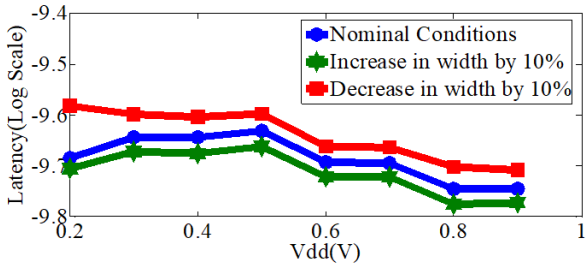

Figure 22.Variation of latency with width variation in unbuffered H tree

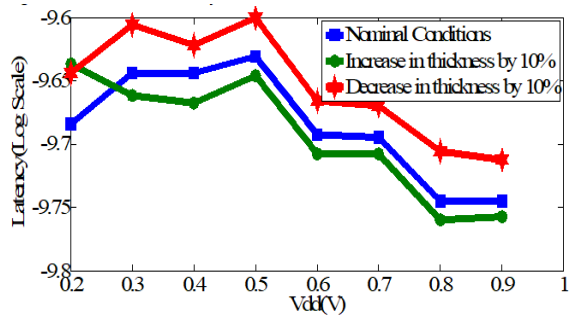

Figure 23.Variation of latency with thickness variation in unbuffered H tree

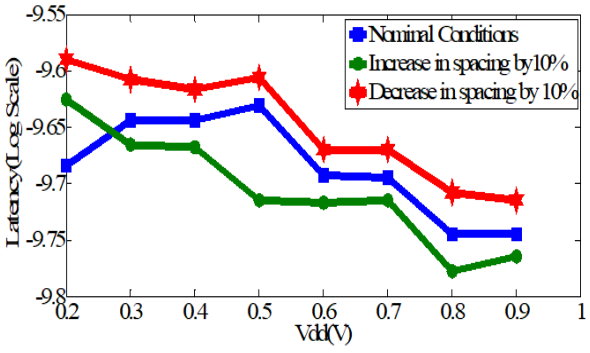

Figure 24.Variation of latency with spacing variation in unbuffered H tree

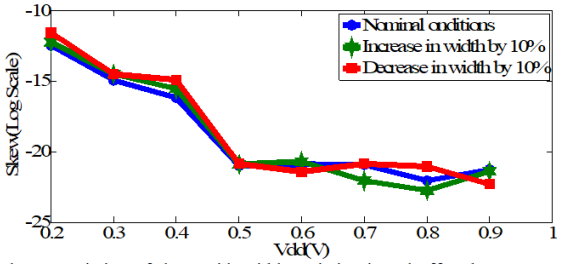

Figure 25.Variation of skew with width variation in unbuffered H tree

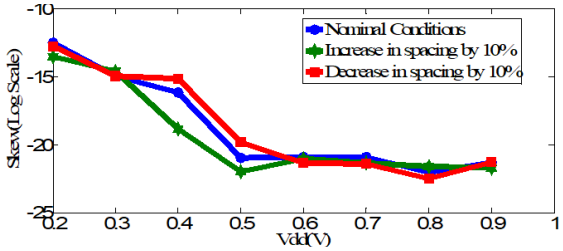

Figure 26.Variation of skew with thickness variation in unbuffered H tree

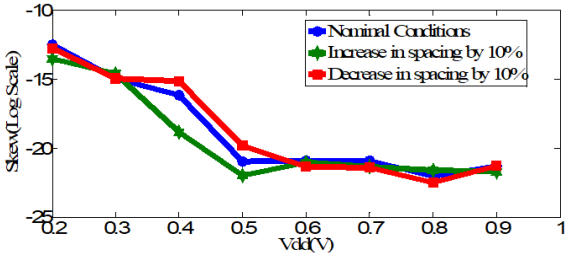

Figure 27.Variation of skew with spacing variation in unbuffered H tree

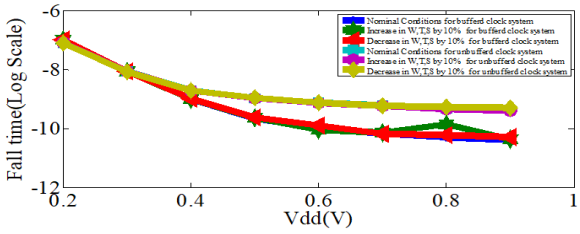

Figure 28.Comparison of fall time of buffered and unbuffered tree under nominal conditions and with Width(W), Thickness(T) and spacing(S) variation

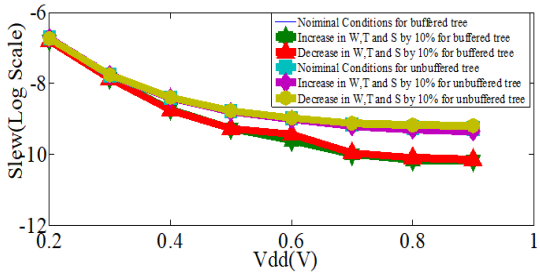

Figure 29.Comparison of slew of buffered and un-buffered tree under nominal conditions and with Width(W), Thickness(T) and spacing(S) variation

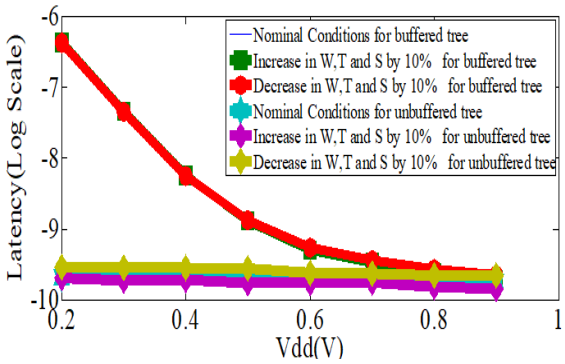

Figure 30.Comparison of latency of buffered and unbuffered tree under nominal conditions and with Width(W), Thickness(T) and spacing(S) variation

Conclusion

The clock system plays a vital role in synchronous digital system. Stability of clock parameters is utmost important in order to ensure the reliable operation of a synchronous system. This paper explored the impact of interconnect parameter variation for clock system with buffered tree and unbuffered tree. The result reveals that even though the interconnect dimension variation have significant impact on clock system parameters in conventional super threshold region, the parameters shows a negligible deviation from their nominal values at 0.2V for buffered tree clock system. The clock system with unbuffered tree also shows small deviation for slew and fall time at 0.2V exhibiting the same performance as with buffered tree. However, the Latency for unbuffered shows a significant deviation at 0.2V for unbuffered tree. Thus, if only interconnect variations are considered then, it can be concluded that the clock system with buffered tree is more robust than with unbuffered tree against interconnect variation in sub threshold regime.

References

1. Reuss RH. Introduction to special issue on circuit technology for ULP. in *Proc. IEEE* 2010; 98(2): 139-143.
2. Paul BC, Agarwal A, Roy K. Low-Power Design Techniques for Scaled Technologies. *Elsevier*, integration, the VLSI journal 2006; 39: 64-89.
3. Zhai B, Blaauw D, Sylvester D et al. Theoretical and practical limits on dynamic voltage scaling. in Design Automation Conf., 2004; 868–873.
4. Calhoun B, Chandrakasan A. Characterizing and modeling minimum energy operation for subthreshold circuits. in Int. Symp. on Low Power Electronics and Designs, 2004; 90-95.
5. Pableand SD, Hasan M. Interconnect Design for Sub-Threshold Circuits. *IEEE transactionson nanotechnology* 2012; 11(3).
6. Soeleman H, Roy K, Paul BC. Robust Sub-threshold Logic for Ultra-Low Power Operation. *IEEE transactions on Very Large Scale Integration* (VLSI) Systems 2000; 9(1).
7. Calhoun B, Ryan J, Khanna S et al. Flexible Circuits and Architechtures for Ultralow Power. *Proceedings of the IEEE* 2010; 98(2).
8. Baker R. CMOS Ciruit Design ,Layout and Simulation. Third Edition, IEEE Press, John Wiley & Sons, Inc. Publication 2010.
9. Wang A, Calhoun BH, Chandrakasan AP. Sub- Threshold Design forUltra Low-Power Systems, 1st ed. *New York*: Springer 2006.
10. Weste N, Harris D. CMOS VLSI Design A Circuits and Systems. Perspective. Fourth Edition Addison-Wesley, Pearson Education.
11. Friedman EG. Clock Distribution Networks in Synchronous Digital Integrated Circuits. *Proc. of IEEE* 2001; 89(5): 665-692.
12. Rabey J, Chandrakasan A, Nikoloic B. Digital Integrated Circuits- A Design Perspective. 2nd Edition, Prentice Hall, New Jersey, USA, 2003.
13. Reuben J, Zackriya M, Harish V et al. A Buffer Placement Algorithm to Overcome Short-Circuit Power Dissipation in Mesh Based Clock Distribution Network. *Engineering Science and Technology an International Journal* 2015; 18: 135-140.
14. T´ellez G, Sarrafzadeh M. Minimal Buffer Insertion in Clock Trees with Skew and Slew Rate Constraints. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 1997; 16(4).
15. Rajaram A, Jiang H, Mahapatra R. Reducing Clock Skew Variability via Cross links. *IEEE Transactions on Computer-Aided of Integrated Circuits and Systems* 25(6).
16. Dave M, Jain M, Baghini M et al. A Variant Tolerant Current Mode Signalling Scheme for On Chip Interconnects. *IEEE Transactions on Very Large Scale (VLSI) Systems* 2013; 21(2).
17. Islam R, Gauthas M. Low Power Clock Distribution Using A Current Pulsed Clocked Flip-Flop. *IEEE Transactions on Circuits and Systems- I Regular Papers* 2015; 62(4).
18. Abdelhadi A, Ginosar R, Kolodny A et al. Timing Driven Variation Aware Synthesis of Hybrid Mesh/ Tree Clock Distribution Networks," Integration, *the VLSI journal* 2013; 46: 382-391.
19. Gaioni L, DeCanio F, Manghisoni M et al. Design and Test of Clock Distribution Circuits for the Macro Pixel ASIC. Nuclear Instruments and Methods in Physics Research, Elsevier, 2015.
20. Tenace V, Miryala S, Calimera A et al. Row Based Body Bias Assignment for Dynamic Thermal Clock-Skew Compensation. *Microelectronics Journal* 2014; 45: 530-538
21. Pable SD, Hasan M. High Speed Interconnect Through Device Optimization for Sub-threshold FPGA. *Microelectronics Journal* 2011; 42: 545-552.

22. Tolbert JR, Zhao X, Lim SK et al. Slew-Aware Clock Tree Design for Reliable Sub-threshold Circuits, ISLPED 2009.
23. Kil J, Gu J, Kim CH. A High - Speed Variation - Tolerant Interconnect Technique for Sub-threshold Circuits using Capacitive Boosting. *IEEE Transactions on Very Large Scale Integration* (VLSI) Systems 2008; 16(4): 456-465.
24. [online]. Available: /http//www.eas.asu.edu/ptm/S